

Application No.: 10/699,691

Docket No.: 20136-00342-US1

**AMENDMENTS TO THE CLAIMS**

This listing of the claims will replace all prior versions and listing of the claims in this application.

**Listing of the Claims:**

Claims 1-3 (canceled)

4. (Currently amended) A method of manufacturing an integrated circuit transformer comprising:

forming a first metallization layer on a substrate comprising a first plurality of turns of a first winding;

forming an insulating layer over said first metallization layer;

forming a second metallization layer on said insulating layer comprising a second plurality of turns of a second winding, and a third plurality of turns of a third windings winding separated by the turns of said second winding and confined to said second metallization layer; and

connection one end of said second winding to one end of said first winding whereby a primary winding is provided ~~for said transformer~~ by said first and second windings on said first and second metallization layer and said third winding comprises a secondary winding for said transformer confined to said second metallization layer.

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5. (Original) The method according to claim 4 further comprising forming a via in said insulating layer and connection said one end of said second winding to said one end of said first winding through said via.

6. (Original) The method according to claim 4 wherein said second plurality of turns of said second winding are separated by said third plurality of turns of said third winding.

7. (Currently amended) The method according to claim 4 further comprising:

forming a fourth set of a plurality of turns ~~of comprising~~ a fourth winding on said first metallization layer to form a ~~second~~ another secondary winding for said transformer.

8. (Original) The method according to claim 7 wherein each turn of said fourth winding is separated from each other by said first plurality of turns of said transformer winding.

9. (Original) The method according to claim 4 further comprising:

forming an insulating layer over a region of a substrate having semiconductor devices; and

forming said first metallization layer on said insulating layer.

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10. (Original) The method according to claim 9 wherein said insulating layer comprises SiO<sub>2</sub>.